REMARKS

Claims 1-18 are pending in the application, of which claims 1, 5, 9, 13 and 14 are independent. Applicant respectfully requests reconsideration of the rejected claims in light of arguments presented below.

The Office Action objects to the abstract of the disclosure for failure to commence on a separate sheet. Applicant accordingly presents the abstract on a separate sheet, with modification in the wording to comply with regulatory limits on length and number of paragraphs. Removal of the objection is respectfully solicited.

The Office Action rejects claims 1-8 under 35 U.S.C. §112, first paragraph, for lack of an enabling disclosure. The Office Action indicates that the specification does not reasonably provide enablement for the limitation of "a time lag one another," as recited in claims 1 and 5.

Applicant amended claim 1, 3-5, 7, and 8 replacing the phrase "a time lag one another" with "time delays that lag one another." Applicant believes the claim amendment clarifies that the signals are changed at points along the time line. Each point has a delay with respect to a reference point, wherein the time delays are lined up and lag one another. We believe that the amendment to claim 1 and similar changes to claims 3-5, 7 and 8 overcome the rejection by relying on claim support in the first example of the disclosure, in pages 24-26 of the specification. Withdrawal of the rejection is respectfully solicited.

The Office Action rejects claims 9-12 under 35 U.S.C. §112, second paragraph, as being indefinite. The Office Action points to the limitation of "... each transfer is performed with a time lag little by little for each bit unit formed of plural bits...," as

recited in claim 9 and considers it indefinite. Applicant accordingly amends claim 9 replacing the phrase "lag little by little" with "delay that lags incrementally." Applicant believes the claim amendment aptly clarifies the way each transfer is performed with a time delay that lags incrementally for each bit unit. This incremental delay defines clearly the way each bit unit, which includes a group of display data of different colors for uniformity of color, lags another unit along the time line. Withdrawal of the rejection is respectfully solicited.

The Office Action rejects claims 9-18 under 35 U.S.C. §103(a) over Shimamoto (U. S. Patent No. 6,147,672). The Office Action admits that Shimamoto fails to specifically teach that the transfer is performed with a time lag little by little for each bit unit formed of plural bits optionally selected from each of the color display data, as recited by claim 9. The Office Action, however, states that it would have been obvious to reduce the transfer time of the display data to the display drivers to provide a more effective countermeasure of electromagnetic interference.

Applicant respectfully asserts that the features of claims 9, 13, and 14 are not disclosed or suggested by Shimamoto. Shimamoto is concerned with converting serial data to parallel bits to accommodate transferring of large number of data bits for high-resolution displays. To the contrary, claims 9 and 13 is directed to serial transfer of data. The delay of each bit unit allows changes to occur at different intervals. In particular, Shimamoto fails to disclose or suggest each transfer performed with a time delay that lags incrementally for each bit unit formed of plural bits optionally selected from each of said color display data, as recited in claim 9. Shimamoto also fails to disclose or suggest a delay unit provided in the display timing control circuit to delay the transfer timing

between one bit unit and another, as recited in claim 13. Contrary to the Office Action's assertion, the reference is silent with regard to any modification or suggestion for changing the prior art display and its drive circuit to arrive at the claimed invention relating to the incremental delay of the data bit units without changing their order or sequence. Although the prior art appears to be concerned with reduction of electromagnetic wave noise, a completely different solution, i.e. conversion to parallel bits, is applied to achieve it. As the bits are in a parallel structure, it would not be possible to introduce a time delay between respective parallel bits. A time delay would only negate the intended solution of Shimamoto. For these reasons, Applicant believes claims 9 and 13 to be patentable over Shimamoto distinct.

As regards claim 14, the Office Action references columns 6-7, lines 56-26, respectively, citing the first and second control circuit of claim 14. The cited portion of Shimamoto relates to the arrangement of the parallel/serial (P-S) converter. There is no disclosure or suggestion of operation with respect to a coincidence of polarity. In particular, there is no disclosure or suggestion of a detector circuit for detecting a coincidence of polarity by comparing a polarity of bit for each predetermined group of image data outputted by the data supply circuit, as claim 14 recites. Nor is there a suggestion of a first and second control circuit for outputting data...when the coincidence of polarity of bit has been detected by the detector circuit, as claim also recites. For these reasons, Applicant believes claim 14 to be patentable.

Accordingly, Applicant believes that claims 9, 13 and 14 and their dependent claims are distinguishable over the prior art and solicits removal of the rejection.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

Date: January 3, 2002

McDERMOTT, WILL & EMERY

David M. Tennant
Registration No. 48,362

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000
Facsimile: (202) 756-8087
SAB:DT:vgp/khb

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1 and 9 were amended as follows:

1. (Amended) An integrated circuit characterized in that multi-port data output signals are generated with respect to a data input signal, and points of changing said data output signals with respect to a time base are set with [a] time delays that lag one another during one period of a reference internal clock signal, so that number of simultaneous changes of display data output signals is reduced.

3. (Amended) An integrated circuit according to claim 1, wherein the points of changing the data output signals with respect to the time base are set to points respectively having [a] time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the data input signal.

4. (Amended) An integrated circuit according to claim 1, wherein the points of changing the data output signals with respect to the time base are set to points respectively having [a] time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the data input signal and by a delay time produced by a delay circuit added to the optional integer times as long as a half period of the data input signal.

5. (Amended) A liquid crystal display characterized in that multi-port display data output signals are generated with respect to a data input signal, and points of

changing said display data output signals with respect to a time base are set with [a] time delays that lag one another during one period of a clock output signal or a reference internal clock signal having a same phase as the clock output signal, so that number of simultaneous chugs of display data output signals is reduced.

7. (Amended) A liquid crystal display according to claim 5, wherein the points of changing the display data output signals with respect to the time base are set to points respectively having [a] time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the clock input signal or the display data input signal.

8. (Amended) A liquid crystal display according to claim 5, wherein the points of changing the display data output signals with respect to the time base are set to points respectively having [a] time delays that lag one another from the active edge of the clock output signal by optional integer times as long as a half period of the clock input signal or the display data input signal and by a delay time produced by a delay circuit added to the integer times as long as the half period of the clock input signal or the display data input signal.

9. (Amended) A driving method of a liquid crystal display characterized in that when red, green and blue color display data composed of plural bits are transferred from a display timing circuit to a TFT drive circuit for driving a TFT liquid crystal panel to display, each transfer is performed with a time delay that lags [little by little] incrementally for each bit unit formed of plural bits optionally selected from each of said display data.